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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/698,622	10/27/2000	Jyh-Ming Jong	P4928/06145.003001	4922

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OSHA & MAY L.L.P./SUN
1221 MCKINNEY, SUITE 2800
HOUSTON, TX 77010

EXAMINER	
BAYARD, EMMANUEL	

ART UNIT	PAPER NUMBER
2631	5

DATE MAILED: 04/15/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/698,622	Applicant(s) JONG ET AL.	
	Examiner Emmanuel Bayard	Art Unit 2631	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 February 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7 and 9-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7 and 9-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This is in response to amendment filed on 2/2/04 in which claims 1-7 and 9-13 are pending and claim 8 is canceled. The applicant's amendments have been fully considered but they are moot based on the new ground of rejection. Therefore this case is made final.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-7 and 9-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tateishi U.S. Patent No 5,790,613 in view of Kamiya U.S. patent No 6,313,686 B1.

As per claims 1 and 9, Tateishi discloses an apparatus for detecting a noise error of a signal comprising: an upper comparator is the same as the claimed (high comparator) (see figs.5, 8-10, 13-15 element 8U1 and col.6, lines 29-30, 45-55) that references a high voltage limit with the signal and generates an output; a low comparator (see figs.5, 8-10, 13-15 element 8L1 and col.6, lines 29-30, 45-55) that references a low voltage limit with the signal and generates an output; and a circuit (see figs.5, 8-10, 13-15 element 88 and col.6, lines 25-67) that processes the high comparator output and the low comparator output, wherein the circuit generates a trigger is considered as the claimed (alarm) if a noise error is detected (see col.7, lines 49-50 and col.8, lines 46-47 and col.10, lines 40-45).

However Tateishi does not teach at least one of the high comparator output and at least one of low comparator output clock the circuit.

Kamiya teaches at least one of the high comparator output and at least one of low comparator output clock the circuit (see fig.1 elements 51 and 52 and col.4, lines 59-67 and col.5, lines 1-7).

It would have been obvious to one of ordinary skill in the art to implement the teaching of Kamiay in Tateishi as to generate a waveform whose harmonic components are made smaller from the junction between the PMOS transistor and the NMOS transistor as taught by Kamiya (see abstract).

As per claim 2, the apparatus of Tateishi does include a high-to-low sub-circuit that detects a noise error during a rising signal transition and a low-to-high sub-circuit that detects a noise error during a falling signal transition (see col.7, lines 45-67 and col.8, lines 43-67 and col.9, lines 43-46 and col.10, lines 10-13 and col.14, lines 10-20).

As per claim 3, the apparatus of Tateishi does include: a plurality of flip-flop circuits (see elements 8U2 , 8L2 and col.6, line 44); a delay buffer (col.6, line 58); and an XOR logic gate (see col.6, lines 58-59).

As per claim 4, the apparatus of Tateishi does include a differential amplifier (see fig.5 element 820).

As per claim 5, the apparatus of Tateishi would include a sense amplifier as to turn off the PMOS transistor from the first stage to change the resistance between the transistor and the power supply.

As per claim 6, the apparatus of Tateishi would include high voltage limit and the low voltage limit is 300 mV as to turn off the PMOS transistor from the first stage to change the resistance between the transistor and the power supply.

As per claims 7 and 13, the apparatus of Tateishi discloses an apparatus for detecting a noise error of a signal comprising: an upper comparator is the same as the claimed (high comparator) (see figs.5, 8-10, 13-15 element 8U1 and col.6, lines 29-30, 45-55) that references a high voltage limit with the signal and generates an output; a low comparator (see figs.5, 8-10, 13-15 element 8L1 and col.6, lines 29-30, 45-55) that references a low voltage limit with the signal and generates an output, wherein the difference between the high voltage limit and the low voltage limit is 300 mV; a high-to-low sub-circuit that detects a noise error during a rising signal transition (see col.7, lines 45-67 and col.8, lines 43-67 and col.9, lines 43-46 and col.10, lines 10-13 and col.14, lines 10-20), wherein the high-to-low sub-circuit comprises, a plurality of flip-flop circuits (see elements 8U2 , 8L2 and col.6, line 44); a delay buffer (col.6, line 58); and an XOR logic gate (see col.6, lines 58-59); a low-to-high sub-circuit that detects a noise error during a falling signal transition (see col.7, lines 45-67 and col.8, lines 43-67 and col.9, lines 43-46 and col.10, lines 10-13 and col.14, lines 10-20), wherein the low-to-high sub-circuit comprises: a plurality of flip-flop circuits (see elements 8U2 , 8L2 and col.6, line 44); a delay buffer (col.6, line 58); and an XOR logic gate (see col.6, lines 58-59) wherein either sub-circuit generates an alarm if a noise error is detected a trigger is considered as the claimed (alarm) if a noise error is detected (see col.7, lines 49-50 and col.8, lines 46-47 and col.10, lines 40-45).

However Tateishi does not teach a plurality of flip-flops clocked at least one of the high comparator output and at least one of low comparator.

Kamiya teaches clocked at least one of the high comparator output and at least one of low comparator. (see fig.1 elements 51 and 52 and col.4, lines 59-67 and col.5, lines 1-7).

It would have been obvious to one of ordinary skill in the art to implement the teaching of Kamiya in Tateishi as to generate a waveform whose harmonic components are made smaller from the junction between the PMOS transistor and the NMOS transistor as taught by Kamiya (see abstract).

As per claim 10, the apparatus of Tateishi would include high voltage limit and the low voltage limit is 300 mV as to turn off the PMOS transistor from the first stage to change the resistance between the transistor and the power supply.

As per claim 11, the apparatus of Tateishi does include wherein the low signal voltage is compared with the low voltage limit by a low-to-high sub-circuit that detects the noise error during a falling signal transition (see col.7, lines 45-67 and col.8, lines 43-67 and col.9, lines 43-46 and col.10, lines 10-13 and col.14, lines 10-20), wherein the low-to-high sub-circuit comprises, a plurality of flip-flop circuits (see elements 8U2 , 8L2 and col.6, line 44); a delay buffer (col.6, line 58); and an XOR logic gate (see col.6, lines 58-59).

As per claim 12, the apparatus of Tateishi does include wherein the high signal voltage is compared with 2 the high voltage limit by a high-to-low sub-circuit that detects the noise error during a falling signal transition (see col.7, lines 45-67 and col.8, lines 43-67 and col.9, lines 43-46 and col.10, lines 10-13 and col.14, lines 10-20), wherein the low-to-high sub-circuit comprises, a plurality of flip-flop circuits (see elements 8U2 , 8L2 and col.6, line 44); a delay buffer (col.6, line 58); and an XOR logic gate (see col.6, lines 58-59).

Conclusion

3. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

McGinn U.S. Patent No 4,796,102 teaches an automatic frequency control system.

Walker U.S. Patent No 5,825,431 teaches a H-sync to pixel clock Phase.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Emmanuel Bayard whose telephone number is (703) 308-9573. The examiner can normally be reached on Monday-Thursday from 8:00 AM - 5:30 PM. The examiner can also be reached on alternate Fridays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad H. Ghayour , can be reached on (703) 306-3034. The fax phone number for this Group is (703) 872-9314.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-3800.

Emmanuel Bayard

Primary Examiner

November 24, 2003